

**HAOPIN MICROELECTRONICS CO.,LTD.**
**Description**

Glass passivated, sensitive gate thyristors in a plastic envelope, intended for use in general purpose switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

Symbol		Simplified outline
		
Pin	Description	
1	Cathode	
2	Anode	
3	Gate	

**Applications:**

- ◆ Motor control
- ◆ Industrial and domestic lighting
- ◆ Heating
- ◆ Static switching

**Features**

- ◆ Blocking voltage to 800 V
- ◆ On-state RMS current to 4 A
- ◆ Ultra low gate trigger current

SYMBOL	PARAMETER	Value	Unit
$V_{DRM}$	Repetitive peak off-state voltages	500R	V
	$V_{RRM}$	600R	
		800R	
$I_T$ (RMS)	RMS on-state current	4	A
$I_{TSM}$	Non-repetitive peak on-state current	35	A

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$R_{th\ j\ -mb}$	Thermal resistance Junction to mounting base		-	-	2.5	K/W
$R_{th\ j\ -a}$	Thermal resistance Junction to ambient	In free air	-	60	-	K/W

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Limiting values in accordance with the Maximum system(IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
$V_{DRM}$	Repetitive peak off-state Voltages	500R 600R 800R	-	500 600 800	V
$I_{TAV}$	Average on-state current	Half sine wave; $Tmb \leq 113^\circ C$	-	2.5	A
$I_{T(RMS)}$	RMS on-state current	All conduction angles		4	A
$I_{TSM}$	Non-repetitive peak On-state current	half sine wave; $T_j = 25^\circ C$ prior to surge	$T=10ms$ $T=8.3ms$	35 38	A
$I^2t$	$I^2t$ for fusing	$T=10ms$	-	6.1	$A^2s$
$DI_T/dt$	Repetitive rate of rise of on-state current after triggering	$I_{TM}=10A$ ; $I_g=50mA$ ; $D_{ig}/dt=50mA/\mu s$	-	50	$A/\mu s$
$I_{GM}$	Peak gate current		-	2	A
$V_{GM}$	Peak gate voltage		-	5	V
$P_{GM}$	Peak gate power		-	5	W
$P_{G(AV)}$	Average gate power	Over any 20 ms period	-	0.5	W
$T_{stg}$	Storage temperature		-40	150	$^\circ C$
$T_j$	Operating junction Temperature		-	125 <sup>2</sup>	$^\circ C$

 $T_j=25^\circ C$  unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Static characteristics						
$I_{GT}$	Gate trigger current	$V_D=12V$ ; $I_T=0.1A$	-	15	200	$\mu A$
$I_L$	Latching current	$V_D=12V$ ; $I_{GT}=0.1A$	-	0.17	10	mA
$I_H$	Holding current	$V_D=12V$ ; $I_{GT}=0.1A$	-	0.10	6	mA
$V_T$	On-state voltage	$I_T=5A$	-	1.23	1.8	V
$V_{GT}$	Gate trigger voltage	$V_D=12V$ ; $I_T=0.1A$ $V_D=V_{DRM(max)}$ ; $I_T=0.1A$ ; $T_j=110^\circ C$	- 0.1	0.4 0.2	1.5 -	V
$I_D$	Off-state leakage current	$V_D=V_{DRM(max)}$ ; $V_R=V_{RRM(max)}$ $T_j=125^\circ C$	-	0.1	0.5	mA

**Dynamic Characteristics**

$D_{VD}/dt$	Critical rate of rise of Off-state voltage	$V_{DM}=67\% V_{DRM(max)}$ ; $Tj=125^\circ C$ ; Exponential wave form; $R_{GK}=100\Omega$	-	50	-	$V/\mu s$
$t_{gt}$	Gate controlled turn-on time	$I_{TM}=10A$ ; $V_D=V_{DRM(max)}$ ; $I_g=5mA$ ; $dI_g/dt=0.2A/\mu s$	-	2	-	$\mu s$
$t_g$	Circuit commutated turn-off time	$V_{DM}=67\% V_{DRM(max)}$ ; $Tj=125^\circ C$ ; $I_{TM}=8A$ $V_R=10V$ ; $dI_{TM}/dt=10A/\mu s$ $dI_g/dt=2V/\mu s$ ; $RGK=1k\Omega$	-	100	-	$\mu s$

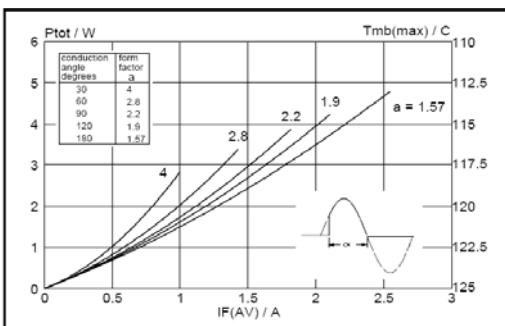
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Fig.1. Maximum on-state dissipation,  $P_{\text{tot}}$ , versus average on-state current,  $I_{T(\text{AV})}$ , where  $a = \text{form factor} = I_{T(\text{RMS})}/I_{T(\text{AV})}$ .

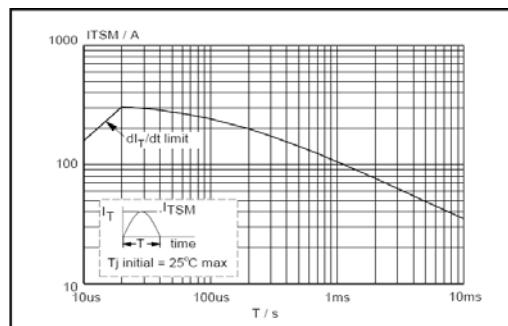


Fig.2. Maximum permissible non-repetitive peak on-state current  $I_{TSM}$ , versus pulse width  $t_p$ , for sinusoidal currents,  $t_p \leq 10\text{ms}$ .

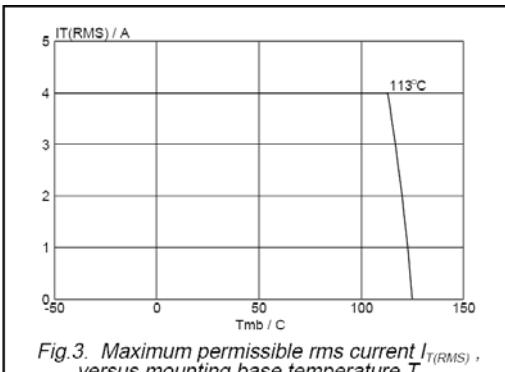


Fig.3. Maximum permissible rms current  $I_{T(\text{RMS})}$ , versus mounting base temperature  $T_{mb}$ .

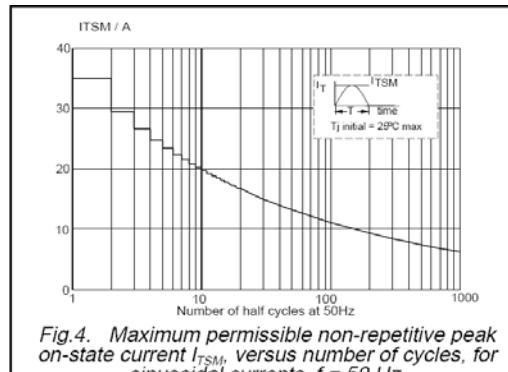


Fig.4. Maximum permissible non-repetitive peak on-state current  $I_{TSM}$ , versus number of cycles, for sinusoidal currents,  $f = 50\text{ Hz}$ .

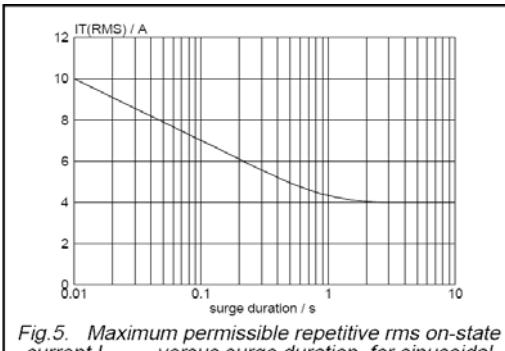


Fig.5. Maximum permissible repetitive rms on-state current  $I_{T(\text{RMS})}$ , versus surge duration, for sinusoidal currents,  $f = 50\text{ Hz}$ ;  $T_{mb} \leq 113^\circ\text{C}$ .

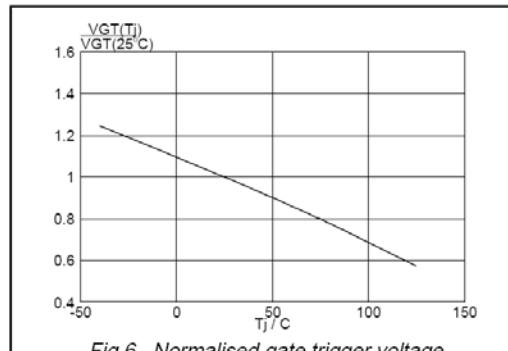


Fig.6. Normalised gate trigger voltage  $V_{GT}(T_j)/V_{GT}(25^\circ\text{C})$ , versus junction temperature  $T_j$ .

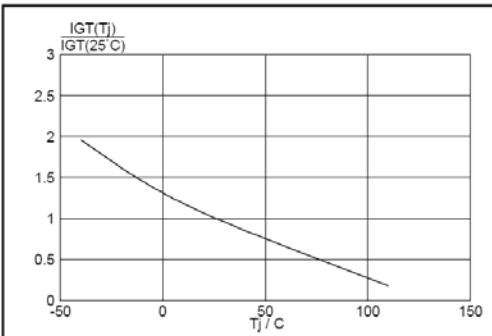
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Fig.7. Normalised gate trigger current  
 $I_{GT}(T_j)/I_{GT}(25^\circ C)$ , versus junction temperature  $T_j$ .

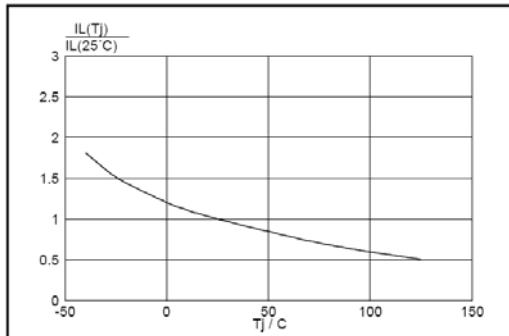


Fig.8. Normalised latching current  $I_L(T_j)/I_L(25^\circ C)$ ,  
versus junction temperature  $T_j$ .

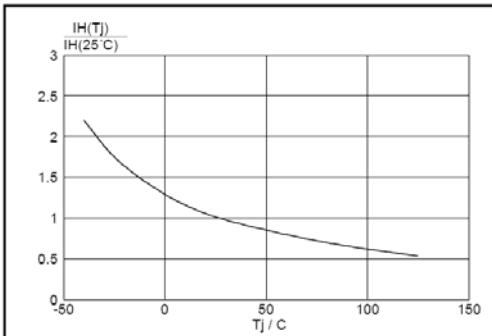


Fig.9. Normalised holding current  $I_H(T_j)/I_H(25^\circ C)$ ,  
versus junction temperature  $T_j$ .

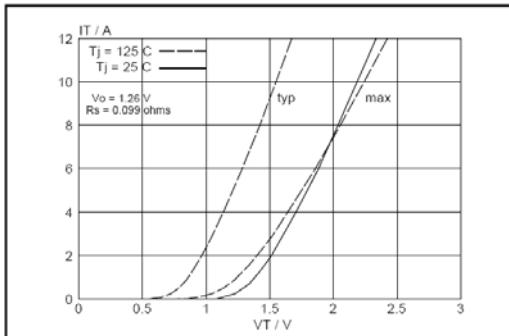


Fig.10. Typical and maximum on-state characteristic.

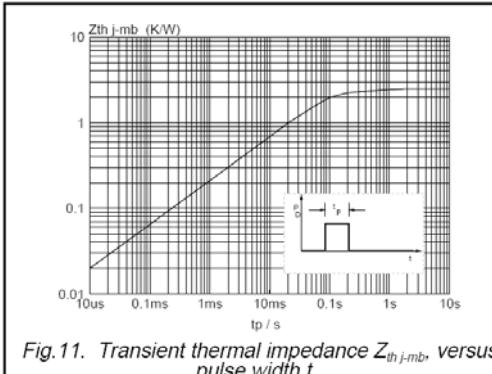


Fig.11. Transient thermal impedance  $Z_{th\ j\ mb}$ , versus  
pulse width  $t_p$ .

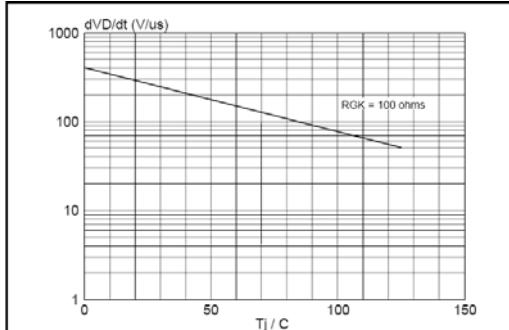


Fig.12. Typical, critical rate of rise of off-state voltage,  
 $dV_d/dt$  versus junction temperature  $T_j$ .

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## MECHANICAL DATA

